Over the last three and half years, the EC-funded III-V-MOS consortium worked to provide device simulation methods and models, integrated into TCAD tools, for successful introduction of optimized III-V n-MOSFET designs in advanced CMOS nodes.

At the end of journey, we report the latest achievements and perspectives.

III-V-MOS: a successful example of integrated modeling approach

Interview of Luca Selmi, III-V-MOS Coordinator

The III-V-MOS project has come to the end. What have been its main achievements?

III-V-MOS has been an intense collaborative experience involving industry and academia. The physics of III-V materials and devices has been tackled at different levels of detail; thanks to that, the III-V-MOS consortium could derive from accurate high-level models computationally affordable TCAD solutions to describe III-V n-MOSFETs. This unique approach led all partners to share precious knowledge, and eventually to deliver a portfolio of new methodologies and simulation tools, starting from atomistic band structure calculations all the way down to advanced full quantum simulations of complete transistors.

How will III-V-MOS have an impact in the future?

Our partners Synopsys and QuantumWise integrated their results into official releases of commercial simulators. Customized setups are thus available to end users for III-V n-MOSFET simulation and optimization in the preferred technology (FD-SOI, FinFET, etc.). Future software releases by our partners will expand further these possibilities in the coming months. Therefore, we achieved not only scientific results published in reviewed journals but also product impact.

Objective 1 > “High level" models for new insights on III-V n-MOS technologies

QuantumWise: DFT modeling of contacts and interfaces

QuantumWise has carried out DFT-NEGF calculations to study the contact resistance between various metals (Ti, Mo, W) and In_{0.5}Ga_{0.5}As and InAs [1]. An example of a device structure is shown at the top of Figure 1. The InGaAs region (right) is much longer than the metal in Figure 1: Top: Ti-InGaAs device structure to study contact resistance. Bottom: Specific contact resistivity vs. doping for Ti-In_{0.5}Ga_{0.5}As interfaces for In and As terminated surfaces (red curves) and for Ti-InAs interfaces (green). The dashed black line is a trend line.
order to properly take into account the weaker screening in the semiconductor. The plot at the bottom shows the calculated specific contact resistivities vs. doping level together with experimental values obtained from the III-V-MOS fabrication partners (IBM and IMEC) and from literature. The contact resistivities were calculated for two different terminations of the In0.5Ga0.5As (either In- or As terminated). As can be seen, the calculated values compare quite closely to the experiments, which brings further trust to both the calculations as well as the experimental procedures.

The methodology to calculate contact resistances is already being used by academic and industrial customers of QuantumWise. Furthermore, the know-how developed in III-V-MOS about atomistic simulation of metal-III-V interfaces are now being continued in the QBiz project (http://qubiz.dk/), on new quantum computing devices and proximity induced super-conductivity at metal-III-V interfaces.


**ETH-Zürich: Study of leakage currents in III-V MOSFETs**

![Figure 2: Minimum sub-threshold swing (right) and drain-induced barrier lowering DIBL (left) of the FinFET and GAA architectures for gate lengths ranging from 8 nm to 20 nm.](image)

Owing to the small bandgap, leakage current in the off-state is a serious concern for III-V MOSFETs, with direct implications on the design of the device. Having clarified that source-to-drain-tunneling (STDT) is the largest contributor to leakage in scaled transistors [2], the performance and leakage mechanisms for different gate lengths in 3D In0.53Ga0.47As FinFETs and Gate All Around (GAA) nanowire FETs have been compared to previous results obtained for 2D ultra-thin body (UTB) FETs using QTX, a non-parabolic-EMA quantum transport solver of ETHZ. The parameters entering the EMA model were fitted to match the lowest conduction bands obtained from atomistic tight-binding calculations for the considered geometries.

**Figure 2** shows the drain-induced barrier lowering, DIBL, and sub-threshold swing, SS, vs. gate length for the FinFET and the GAA architectures. As expected, the GAA shows significant advantages over the FinFET due to the better electrostatic control originating from the 4th gate in the bottom of the device and the reduced height. While both architectures suffer from a substantial increase in STDT leakage at gate lengths below 15 nm, the better electrostatic control of the GAA architecture gives it a clear advantage compared to the FinFET architecture. We found that the FinFET architecture does not present significant improvements compared to the 2D UTB FET due to the large fin height, which strongly reduces the 3rd gate’s control. Increasing the effective channel lengths by introducing a gate underlap is an effective technology option to limit the STDT leakage while keeping the benefits of high mobility of III-V materials.

[2] Second III-V-MOS newsletter, [https://www.iii-v-mos-project.eu](https://www.iii-v-mos-project.eu)

**Objective 2 > Advances in TCAD for III-V MOSFETs**

**IUNET and Synopsys: Quasi-ballistic transport models for ultra-thin-body InGaAs MOSFETs**

IUNET-Bologna has recently developed an approach for including quasi-ballistic effects into TCAD drift-diffusion simulations of short-channel III-V ultra-thin-body (UTB) double-gate (DG) MOSFETs. The quasi-ballistic mobility model works as follows: in the linear (low longitudinal field) regime a ballistic mobility term is computed consistently with the electrostatic potential profile provided by TCAD simulations and then combined in each point within the channel with a standard TCAD drift-diffusion model.
mobility model through a Matthiessen-like rule; at high-fields, the Canali model is used to account for velocity saturation effects, using $v_{\text{sat}}$ and $\beta$ as fitting parameters. The Sentaurus Device simulations use the Modified Local Density Approximation (MLDA) model to account for quantization in the transverse confined direction. The full procedure has been implemented in Synopsys Sentaurus through a custom library [3].

An In$_{0.53}$Ga$_{0.47}$As DG UTB 15-nm gate-length template device with 7-nm channel thickness has been used for benchmarking and calibration against Multi-Subband Monte Carlo simulations by IUNET-Udine (Figure 3). As expected, the standard TCAD without QB corrections largely overestimates the MSMC currents. The TCAD currents obtained with the developed mobility model for three different gate lengths (15 nm, 30 nm and 70 nm) show a much better agreement with MSMC results over most of the gate bias range for all devices (Figure 4). A TCAD friendly version of this model has been included in recent releases of the Synopsys SDevice [4].

**IMEC: TCAD requirements for In$_x$Ga$_{1-x}$As device design and optimization**

Investigating new device architectures beyond FinFETs, most likely focused on gate-all-around (GAA) devices, and studying devices with different Indium contents will be major paths for III-V n-MOSFET performance optimization at IMEC. For TCAD this means that systematic predictions as a function of In-content are needed. The first essential step is thus full band structure calculation including non-parabolicity effects and up to high energy, as available in the empirical pseudopotential tool Sband. Based on that pseudopotential table, the TCAD tool for the prediction of the In-dependence of device performance is the full-band Monte Carlo device simulator Sentaurus Monte Carlo.

The band structure effect is illustrated in Figure 5 which shows the velocity profiles in an InGaAs SOI-FinFET (and the corresponding DOS in the inset) using either a pseudopotential band structure or an analytic non-parabolic band model (with an effective mass of 0.05 $m_0$ and a nonparabolicity factor of 0.8 1/eV). Note that the analytic band model overestimates the on-current by almost 20 % due to an underestimation of the DOS at higher energies. Of course, also other features are needed for complete III-V device simulation at TCAD level: a) Fermi-Dirac statistics; b) quantum-correction based on Schrödinger-Poisson solutions including wavefunction penetration into the oxide (since density-gradient cannot reproduce this, [5]); c) trap-induced Fermi level pinning [5] and d) contact resistance [6].

These have been provided within III-V MOS. For further analysis such as on variability with the impedance-field method for given device type and In content, drift-diffusion simulations with a ballistic mobility model [4] will be applied at IMEC. As reference in simplified device structures, subband Boltzmann and NEGF solutions might be used to validate or calibrate the TCAD tools. In the coming years, development of III-V devices will therefore rely on TCAD support with the aforementioned Monte Carlo and drift-diffusion capabilities as provided within the III-V MOS project.


**Figure 4:** Current vs. gate voltage for different In$_x$Ga$_{1-x}$As devices with 7-nm channel thickness and 30 nm gate length. The currents obtained with the developed mobility model for three different gate lengths (15 nm, 30 nm and 70 nm) show a much better agreement with MSMC results over most of the gate bias range for all devices (Figure 4).

**Figure 5:** Velocity profiles in an InGaAs SOI-FinFET with 20 nm gate length and 7 nm spacer width using a pseudopotential or an analytic nonparabolic band structure with on-currents of 389 and 463 µA/µm, respectively.
Objective 3 > Identify most promising device architectures and optimized designs.

IUNET and ETHZ: Design and benchmarking of device performance and strain effectiveness in III-V MOSFETs

The performance assessment of III-V FETs has been a prominent objective of the III-V-MOS project. The performance and scalability of In$_{0.53}$Ga$_{0.47}$As double-gate ultra-thin-body (DG-UTB), triple-gate FinFET, and gate-all-around nanowire (GAA NW) field-effect transistors (FETs, Figure 6), have been evaluated for two technology nodes with $L_G=15$ nm at $V_{DD}=0.63$ V and $L_G=10.4$ nm at $V_{DD}=0.59$ V and 0.5 V. The analysis has been carried out with different simulation methodologies, including several scattering mechanisms and the impact of series resistance, $R_{SD}$.

First, ballistic simulations have been performed with a state-of-the-art Non-Equilibrium Green’s Function (NEGF) quantum transport tool relying on either the effective mass approximation (EMA) for the 3-D structures or on the empirical nearest-neighbour tight-binding (TB) method for the planar ones. In case of EMA simulations, the effective masses have been calibrated using full-band data and the strong non-parabolicity of In$_{0.53}$Ga$_{0.47}$As has been fully taken into account [9].

The $I_D$-$V_{GS}$ transfer characteristics of the simulated III-V devices are reported in Figure 7 for the technology nodes mentioned above. A $<110>$-oriented strained-Si GAA NW FET with the same dimensions as its III-V counterpart has also been investigated to serve as a reference. The OFF-currents of all logic switches have been set to 100 nA/µm. It has been found that the ON-current values of all III-V devices at all nodes are relatively homogeneous, that they are higher than in strained-Si, and that the GAA NW is the architecture that benefits the most from the scaling of the dimensions, particularly in terms of the analog figures of merit.

At $V_{DD}=0.5$ V, a relevant supply voltage to benchmark any new technology, the III-V GAA NW FET significantly outperforms the strained-Si device as it exhibits a more than two times smaller switching time, a three times lower switching energy, thrice the cutoff frequency, and nearly twice the intrinsic gain. These

Figure 6: Schematic view of the (a) DG-UTB, (b) triple-gate FinFET, and (c) gate-all-around nanowire architectures investigated in III-V-MOS. All have an In$_{0.53}$Ga$_{0.47}$As channel.

Figure 7: Full-quantum $I_D$-$V_{GS}$ characteristics at $V_{DS}=V_{DD}$ (ballistic for III-V and with electron-phonon scattering for the strained-Si GAA NW FET) for (a) $L_G=15$ nm, (b) $L_G=10.4$ nm at $V_{DD}=0.59$V, and (c) $L_G=10.4$ nm at $V_{DD}=0.5$V. Data for the III-V DG-UTB (black dotted lines), III-V triple-gate FinFET (dashed blue lines), III-V GAA NW (dash-dotted red lines), and strained-Si GAA NW (green lines) are presented.

Figure 8: Simulated drain current for the DG -UTB FET with $L_G=15$ nm and $V_{DD}=0.63$ V.
promising results, presented at the IEDM 2016 conference in San Francisco [10], highlight the clear advantages of III-V compounds at advanced technology nodes, where they sustain slightly higher currents than strained-Si at much lower inversion charges.

To more accurately assess the performance of III-V devices, it is however important to go beyond the ballistic limit of transport. Figure 8 reports the I-V characteristics for DG-UTB template transistors with \( L_G = 15 \) nm and illustrates the impact of different refinements in the transport model. Simulations were obtained with the Multi-Subband-Monte-Carlo approach developed in IUNET-Udine [11,12], and scattering models have been calibrated to reproduce experimental mobility data by IBM. As can be seen the inclusion of scattering significantly lowers the on-current, which is further reduced by the inclusion of \( R_{DS} \). Our results demonstrate that III-V transistors are scalable and their application will not be restricted to a single technology node.

Strain induced performance enhancements in InAs and InGaAs FETs has also been thoroughly investigated ranging from band-structure to complete device level simulations. Even if modolation of the effective masses by strain is not negligible, the changes in the non-parabolicity factors tend to compensate the changes in masses. Different calculation methods were found to provide somewhat different strain induced modulations of band-structure parameters, hence Figure 9 compares the ballistic \( I_{DS} \) versus \( V_{GS} \) curves for the \( L_G = 10.4 \) nm bandstructure parameters extracted from tight-binding (open symbols) or \( k \cdot p \) calculations (closed symbols). In both cases the \( I_{DS} \) versus \( V_{GS} \) curves show a modest sensitivity to strain, making us confident that our results are fairly robust against the uncertainties in the bandstructure parameters. Our results suggest that strain induced performance enhancements in ideal trap-free III-V based n-FETs are not as rewarding as they have been for silicon FETs.

![Figure 9](image)

**Figure 9:** Simulated, ballistic drain current for the DG-UTB FET with \( L_G = 10.4 \) and \( V_{DD} = 0.59 \) V nm either for relaxed or for strained InAs.

UTB-SOI template by using either the \( k \cdot p \) or \( k \cdot p \) calculations (closed symbols). In both cases the \( I_{DS} \) versus \( V_{GS} \) curves show a modest sensitivity to strain, making us confident that our results are fairly robust against the uncertainties in the bandstructure parameters. Our results suggest that strain induced performance enhancements in ideal trap-free III-V based n-FETs are not as rewarding as they have been for silicon FETs.


### IUNET-UniMoRe: Variability/sensitivity analysis in III-V MOSFETs

Short-range statistical variability and long-range systematic process variations are both of utmost importance to define the specifications of manufacturable nanoscale devices at advanced CMOS nodes. III-V-MOS partner IUNET-UniMoRe devoted extensive simulation studies to these aspects in the project.

InGaAs DG-UTB and FinFET MOSFETs at the 15 nm and 10.4 nm channel length nodes were scrutinized by means of Sentaurus Device 3D numerical simulations with models for III-Vs developed in the project [13]. 15-nm Si-based devices have been simulated as well for comparison. Statistical variability was evaluated for random dopant fluctuations, gate-metal workfunction fluctuations, gate line edge roughness, and body-surface or fin-sidewall roughness by the impedance field method. Uniform variations were instead applied to critical device dimensions and doping profiles to assess the sensitivity to long-range, systematic process variations.

According to our analysis, see Figure 10, InGaAs FETs show higher threshold-voltage (\( V_t \)) variability than Si ones but smaller normalized ON-current variability. Furthermore, InGaAs devices exhibit worse \( V_t \) sensitivity to systematic process variations than Si FETs. Nonetheless, total \( V_t \) variability appears manageable at the 15-nm node, with an overall predicted \( \sigma(V_t) < 30 \) mV considering the combined effect of all variability sources and \( \pm 10\% \) errors on gate length and channel thickness. It is also not significantly affected by scaling to the 10.4-nm node, provided that IRTS

![Figure 10](image)

**Figure 10** Comparison of total \( \sigma(V_t) \) sensitivity to gate length (top) and channel thickness (bottom) for InGaAs and Si UTB-DG and FinFET structures at node \( (L_G = 15 \) nm, \( V_{DD} = 0.63 \) V, Fig.6). The star corresponds to experimental data from a 14-nm Si FinFET process [14].
predictions about line-edge-roughness improvements are met. Scaling influences both $V_t$ and $\sigma(V_t)$ sensitivities to channel-thickness variations, the combination of the two actually being the most critical issue for InGaAs device scaling as far as variability/sensitivity aspects are concerned.


Objective 4 > Transfer of technologies and knowledge

**Synopsys, IMEC, IBM and GLOBALFOUNDRIES: Accelerating III-V on Silicon technology development by TCAD**

Exploitation of project results has already started, especially by QuantumWise and Synopsys, with numerous software releases incorporating III-V-MOS models and calibrations (Synopsys’s releases J-2014.09, K-2015.06, L-2016.03, and M-2016.12). Furthermore, the simulation methodology and the TCAD models for III-V MOSFETs elaborated in the project have been transferred into IBM, IMEC and GLOBALFOUNDRIES environments, in the form of a set of simulation setups for FD-SOI- and Bulk-FinFETs within the Sentaurus TCAD suite from Synopsys. Customization of the setups has been carried out and the usability of the simulation tools has been assessed. The developed TCAD simulation environment features run times for a complete IV curve that are in the expected and needed time frame for industrial applications. A further release by Synopsys is foreseen later this year (N-2017.09).

III-V-MOS awards: International recognition for our work

- The **best Student Paper Award of the VLSI Technology Symposium 2016** was received at the 2017 edition of the conference by Lukas Czornomaz, IBM Zurich, for the paper entitled “**First Demonstration of InGaAs/SiGe CMOS Inverters and Dense SRAM Arrays on Si Using Selective Epitaxy and Standard FEOL Processes**”.

- The contribution entitled “**Improved surface roughness modeling and mobility projections in thin film MOSFETs**”, by O. Badami, et al. from IUNET-Udine received the **ESSDERC 2015 Best Paper Award**. The paper discusses new non-linear model of surface roughness scattering that for the first time reconciles the r.m.s. of the surface roughness with measured values in both III-V and Si.

IBM receives the CS Industry Innovation Award

- Scientists at IBM Research GmbH received the **2017 Compound Semiconductor Industry Innovation Award**. The recognition is a culmination of five years of research by the Zurich-based IBM team, III-V-MOS partner, which is focused on using high mobility materials into silicon CMOS technology to scale below the 7 nanometers nodes. While a few approaches have been proposed, the IBM team’s winning work is the only one that reports basic building blocks of digital circuits at relevant dimensions and achieves a major milestone towards a manufacturable hybrid InGaAs/SiGe CMOS technology. It is based on three key features in a single technology: the selective growth of high quality InGaAs-on-Insulator regions, the fabrication of InGaAs finFETs with physical gate length $L_g=35$ nm with good device characteristics, and the processing of functional 6T-SRAM cells with a cell area $\approx 0.4\mu m^2$.

III-V-MOS has contributed and also received benefit from these demonstrations. Test structures and complete devices were made available to III-V-MOS for dedicated experiments and model pre-calibration. Over the last three and a half years, an intense collaboration between experimental and modelling partners yielded accurate TCAD models calibrated on the partners’ hardware, which could then be used to improve the device performance. In particular, it was found that the sidewall spacers should be made thinner and the extension regions should be underlapped by a few nanometers from the gate edge. This study significantly accelerated the development of the InGaAs MOSFET technology.